IN THE CLAIMS:

1-10. (Cancelled)

11. (Currently Amended) The multi-word arithmetic device of Claim [[10,]] 19 wherein, in processing (2) and (3), the arithmetic unit selects sets of word pairs, each set formed from all the pairs of words that generate a partial product with a same digit position, sets input values in the multiplier, and computes and accumulates the partial products for the selected pairs of words in sequence from the set with a lowest digit position.

12. (Original) The multi-word arithmetic device of Claim 11, wherein, in processing (2) and (3), the arithmetic unit stores in the memory as part of a multiplication result a lower word from a two-word accumulated result obtained by accumulating partial products with the same digit position, and adds an upper word from the accumulated result to partial products that have a digit position one word higher and are thus the next to be calculated.

13. (Original) The multi-word arithmetic device of Claim 12, wherein the arithmetic unit performs an operation for storing a lower word from the accumulated result in the memory simultaneously with an operation for adding an upper word from the accumulated result to partial products that have a digit position one word higher and are thus the next to be calculated.

14. (Currently Amended) The multi-word arithmetic device of Claim [[10,]] 19 wherein, when computing and accumulating partial products in processing (2) and (3), the arithmetic unit updates accumulated values by (a) simultaneously (i) computing a partial product and (ii) reading a previously accumulated one-word value from the memory, (b) adding the

accumulated one-word value to a corresponding word in the partial product, and (c) storing a result of the addition in a corresponding area of the memory.

15-18. (Cancelled)

19. (New) A multi-word arithmetic device for executing modular arithmetic on multi-word integers, in accordance with instructions from an external device, the multi-word arithmetic device comprising:

a memory;

an arithmetic unit for executing, on word units, at least two types of word calculations, including addition and multiplication, and outputting a one-word calculation result;

a memory input/output circuit for performing (1) a first data transfer for storing in the memory at least one integer received from an external device, (2) a second data transfer for inputting at least one integer stored in the memory into the arithmetic unit in word units, (3) a third data transfer for storing in the memory the calculation result output from the arithmetic unit, and (4) a fourth data transfer for outputting the calculation result from the memory to the external device; and

a control circuit for, according to instructions received from the external device,

(a) specifying, to the memory input/output unit, data to be transferred by the second and third data transfers, and

(b) specifying, to the arithmetic unit, a type of word calculation to be executed,

thereby controlling:

(i) the arithmetic unit to selectively perform one of at least two types of modular arithmetic on the at least one integer stored in the memory; and

(ii) the memory input/output circuit to store the calculation result of the modular arithmetic into the memory,

wherein the selected modular arithmetic includes a plurality of word calculations, each word calculation for a different word of the at least one integer;

when the selected modular arithmetic is performed, the control circuit repeatedly instructs, for each word of the at least one integer, the arithmetic unit to perform the word calculation,

wherein the at least two types of modular arithmetic include Montgomery reduction calculating a residue for A·R^(-l) mod P, when each word has k bits, A is a 2n-word integer used for input data, R is an integer 2^(kxn) and P is an n-word integer; and

upon receiving, from the external device, an instruction to execute Montgomery reduction and an indication of a number of words 2n for an integer A on which Montgomery reduction is to be performed, the control circuit controls the memory input/output circuit and the arithmetic unit to execute Montgomery reduction,

wherein, when receiving an instruction to execute Montgomery reduction from the external device, the control circuit controls the memory input/output circuit and the arithmetic unit so as to execute the following processing:

(1) the memory input/output circuit acquires integers A, P and V from the external device and stores the obtained integers in the memory, the integer V being -P^(-l) mod R;

(2) the arithmetic unit computes partial products for words from each of (i) a lower n words of the integer A stored in the memory, and (ii) the integer V, and accumulates words in partial products having a same digit position, repeating the process sequentially from a lowest word in each integer until n words of accumulated results are obtained, and storing the accumulated results in the memory as a piece of n-word intermediate data B;

(3) the arithmetic unit computes partial products for words from each of (a) the piece of intermediate data B and (b) the integer P stored in the memory, and accumulates words in the partial products having a same digit position so that, when a lowest word is a 0th word, accumulated results for a 0th to (n-3)th word are not obtained, but accumulated results for a (n-2)th word to a (2n-l)th word are obtained and stored in the memory as the upper (n+l) words of a piece of intermediate data D;

(4) the arithmetic unit (a) generates (i) a carry obtained from a one-word addition performed by adding a lowest word from each of the piece of intermediate data 0 and an integer AA, and (ii) a one-bit logical value, the integer AA being an upper (n+l) words of the integer A, and the one-bit logical value being 0 when a one-word addition result is 0, and 1 when the one-word addition result is not 0, and (b) adds an upper n words of the piece of intermediate data D, an upper n words of the integer AA, the carry and the one-bit logical value, by repeating addition of word units sequentially from a lowest word in each integer, while propagating a carry, until n words of data are obtained, and stores an addition result in the memory as a piece of n-word output data M; and

(5) when the output data M stored in the memory is at least as large as the integer P, the arithmetic unit subtracts the integer P from the output data M until the output data M is 0 or a positive integer smaller than the integer P, by repeating subtraction of word units

sequentially from a lowest word in each integer, while propagating a carry, until n words of data are obtained, and stores the subtraction results in the memory as a new piece of n-word output data M,

wherein in processing (4), the arithmetic unit adds a piece of one word data containing all ones to the piece of intermediate data D and the integer AA, and stores an upper n words of an obtained addition result in the memory as the output data M.